A 145μW 8×8 Parallel Multiplier
based on Optimized Bypassing Architecture

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Abstract— **A low-power parallel multiplier based on optimized bypassing architecture (OBA) is proposed. The proposed OBA has two kinds of adder cells to reduce power consumption by 15.7 %. One is the two-dimensional bypassing adder (TDBA) which performs both row and column bypassing scheme simultaneously, and the other is the modified row-bypassing adder (MRBA) for the proposed row-bypassing scheme. In the proposed TDBA and MRBA, the logic evaluation is partially activated by internal tri-state buffers (ITBs) in order to save the switching power dissipation up to 33.7 % and 32.0 %, respectively. Implemented in 0.13 μm CMOS process, the proposed 8×8 parallel multiplier consumes only 145 μW.**

I. INTRODUCTION

Recently, low power Digital Signal Processing (DSP) technology is widely used in battery-powered mobile devices for the graphics and MODEM applications. Especially, the multiplier is the critical arithmetic operation unit for many DSP applications, such as filtering, convolution, Fast Fourier Transform (FFT), etc. For example, power consumption of multipliers is about 30% of the 64-point radix-4 pipelined FFT processor [1].

The power dissipation in digital CMOS circuits can be divided into static and dynamic power dissipation as in (1).

$$P = \alpha f_c C_L V_{DD}^2 + I_{SC} V_{DD} + I_{leakage} V_{DD}. \qquad (1)$$

While α is switching probability, f_c is the clock frequency, C_L is the load capacitance, V_{DD} is the supply voltage, I_{SC} is the short circuit current, and $I_{leakage}$ is the leakage current. Although the proportion of short circuit current and leakage current in cutting-edge CMOS process is not negligible, the dynamic power consumption of the multiplier is much more dominant in over 0.13 μm CMOS processes. From (1), the power consumption can be reduced by decreasing the number of switching activities.

Many previous works tried to reduce the switching activity of the multiplier [2-7]. Among them, the bypassing scheme disables the operations in some rows or columns to save the switching power consumption [4-5]. The row-bypassing multiplier [4] uses additional tri-state buffers and MUXs to skip the full adder (FA) cell in the row of zero bits. Fig. 1 (a) shows the structure of conventional 4×4 row-bypassing
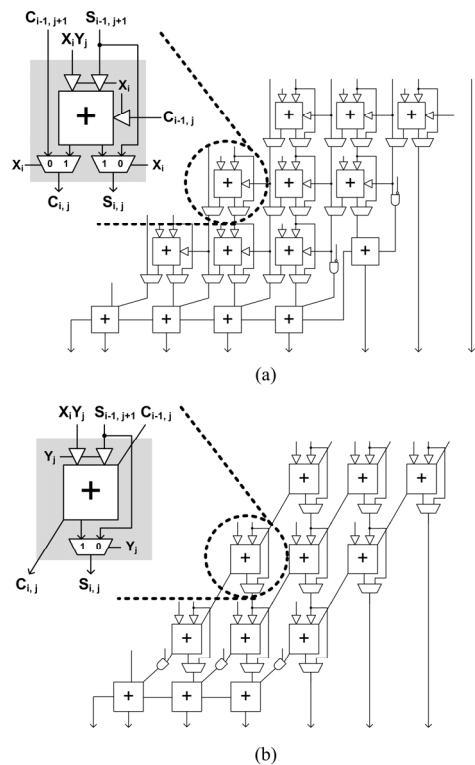

Figure 1.   Structures of 4×4 (a) row-bypassing multiplier [4] and (b) column-bypassing multiplier [5]
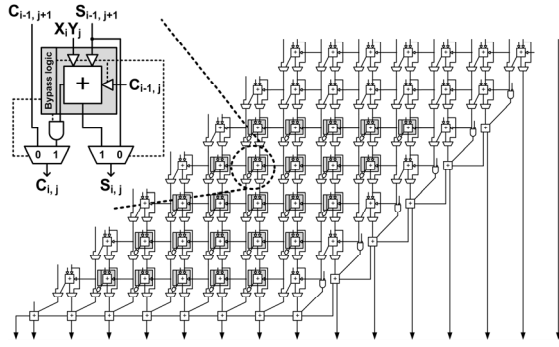
Figure 2. Structure of 8×8 2-dimensional bypassing multiplier [6]

multiplier. Similarly, the column-bypassing multiplier [5] uses additional tri-state buffers and MUXs to skip FA cell in the column of zero bits. As shown in the Fig. 1 (b), the column-bypassing multiplier has less logic than the row-bypassing multiplier because column-bypassing does not need to consider bypassing of the carry bit. In [6-7], the 2-dimensional bypassing multiplier is proposed which detects the nullity of the partial products and the bit of multiplicand to determine whether FA cells on the corresponding row and column are skipped or not, respectively. Fig. 2 shows the structure of the 8×8 2-dimensional multiplier [6]. The adder cells of 2-dimensional bypassing multiplier have additional logics to solve the conflict which appears when row-bypassing and column-bypassing occur simultaneously. The additional logics take large circuit overhead.

In this paper, a low power parallel multiplier based on optimized bypassing architecture (OBA) is proposed. To reduce the power consumption and to avoid the conflict that occurs when using both row-bypassing and column-bypassing, the OBA with two kinds of adder cells, two-dimensional bypassing adder (TDBA) and modified row-bypassing adder (MRBA), is adopted. Each adder cell does not have any FAs

to reduce circuit overhead, and logic evaluation is partially activated to reduce power dissipation.

The rest of this paper is organized as follows. Section II explains the OBA of the proposed multiplier. In Section III, the circuits of TDBA and MRBA are described in detail. Implementation results are shown in Section IV. Finally, Section V concludes the paper.

II. OPTIMIZED BYPASSING ARCHITECTURE (OBA) OF THE PROPOSED MULTIPLIER

Fig. 3 (a) shows the proposed optimized bypassing architecture (OBA) which is an optimized architecture for low-power parallel multipliers. The OBA is composed of two kinds of adder cells: TDBA and MRBA. The TDBA is an adder cell which simplifies both row and column bypassing scheme, and the MRBA is an adder cell which modifies the row-bypassing scheme. With the proposed OBA, the power consumption of the multiplier is much lower than that of multipliers with conventional 2-dimensional bypassing or row-bypassing architectures.

In the proposed TDBA, input signals skip the logic gates when either the row or column bit is zero. Also, the TDBA has less logic gates than the previous adder cells with 2-dimensional bypassing scheme [6-7]. So it can reduce power consumption. However, if the whole multiplier is made by the TDBA, there is a carry problem caused by conflicts between the row-bypassing and the column-bypassing when they simultaneously applied together. For example, in Fig. 3 (b), when both row input X_2 and column input Y_1 are 0 and the carry input $C_{1,2}$ is 1, the carry output $C_{2,1}$ is 1 due to bypassing. If X_3 is 1, $C_{3,1}$ is not 1 but 0 by the column-bypassing scheme because Y_1 is 0. The lost carry bit $C_{2,1}$ makes errors in the multiplication. Therefore, the OBA has TDBAs only on the first and the last columns and the first two rows, in which the carry problem does not occur, as shown in Fig. 3 (a). The remaining part of the multiplier should be different type of

(a)   (b)
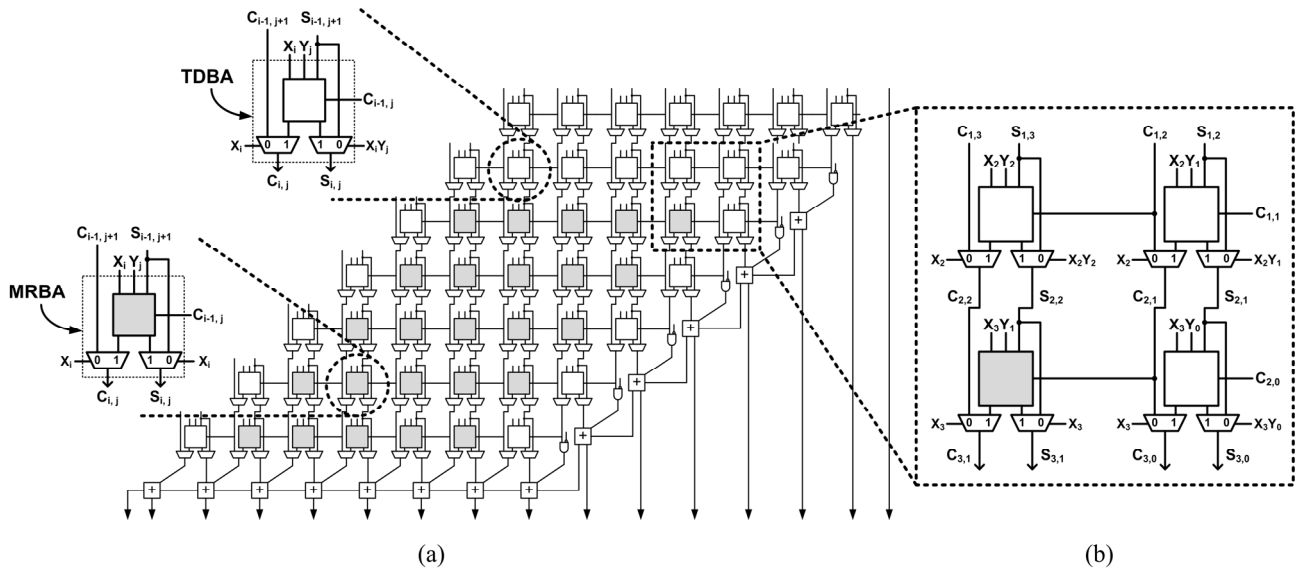
Figure 3. (a) Overall structure of proposed 8×8 multiplier (b) example of the carry problem

adder cells unlike TDBAs.

In the previous works on 2-dimensional bypassing [6-7], bypass logic is added to the adder cell to solve the carry problem. Adder cells, on the region where the carry problems can occur, contain the bypass logic which generates control signals using inputs and carries of its predecessor cells. However, the logic equation of the bypass logic [6] is quite complicated, and thus the bypass logic takes large power and area overhead.

The OBA adopts the MRBAs instead of 2-dimensional bypassing adder cells with bypass logic. The MRBA does not make the carry problem and has less logic gates than the adder cell with bypass logic. In fact, when carries of predecessor cells are considered to solve the carry problem, the output of the adder cell is the same as the output of the adder cell with row-bypassing scheme. Thanks to the proposed MRBA, the carry problem can be solved with low-power consumption.

III. CIRCUIT DETAILS OF ADDER CELLS

A. Two-Dimensional Bypassing Adder (TDBA)

In the previous works of 2-dimensional bypassing [6-7], the adder cell which has both row and column bypassing scheme consists of a FA and additional logics. As shown in Fig. 4 (a), since the truth table of the TDBA is very simple, it can be simplified with some logic gates instead of using FA and several logics. By doing so, it can reduce the power and area overhead. Moreover, the TDBA uses 4-transistor type XNOR gate with cascaded inverter for driving output [8] to reduce the power consumption.

In the TDBA, logic evaluation is disabled with internal tri-state buffers (ITBs) when the logic is not used to eliminate the unnecessary switching power consumption. Fig. 5 shows the circuit schematic of the TDBA. As shown in the Fig. 5, ITBs are added to the 2-input NAND gate and inverters in front of MUXs. When the row input X is 1, the output C_{out} depends on the column input Y as shown in Fig. 4 (a), so MUX which uses Y as a control bit should be necessary. However, when the ITB is used, the output node of the inverter is floated, and thus MUX can be replaced by one transistor. Hence, using
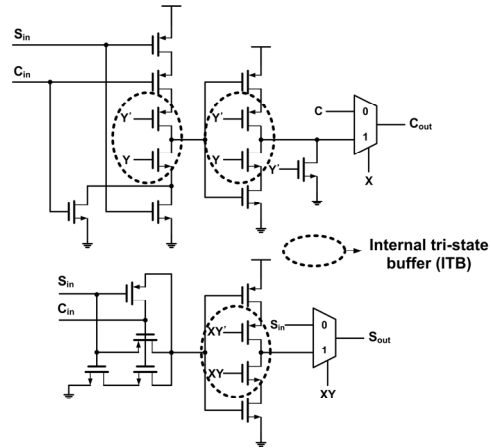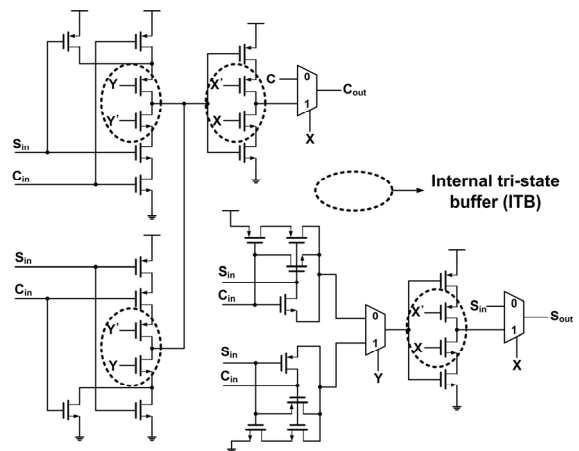

Figure 5.   Circuit schematic of TDBA
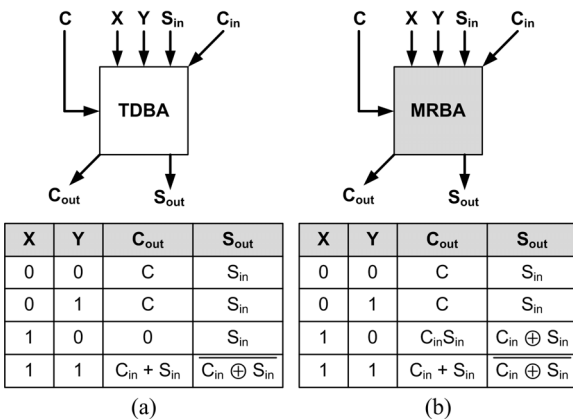

Figure 6.   Circuit schematic of MRBA

ITBs, the power consumption can be reduced.

B. Modified Row-Bypassing Adder (MRBA)

The MRBA is modified version of the adder cell used in the row-bypassing multiplier [4]. As same as the TDBA, the MRBA consists of some logic gates rather than FA. The truth table of the MRBA is shown in Fig. 4 (b). To save the switching power consumption in the MRBA, ITBs are used to suspend logic evaluation in unnecessary cases. Fig. 6 shows the circuit schematic of the MRBA. The ITBs are added to the 2-input NAND gate, 2-input NOR gate, and inverters in front of MUXs. XOR and XNOR gates used in the MRBA are 4-transistor type with cascaded inverter for driving output [8] to reduce power consumption like TDBA. In the MRBA, one MUX can be removed by the similar reason as the TDBA. When the row input X is 1, the output C_{out} depends on the column input Y. However, a MUX with a control bit Y can be eliminated because the output nodes of the NAND and NOR gates are floated alternatively.

IV. IMPLEMENTATION RESULTS

The proposed multiplier based on OBA is implemented in 0.13 μm CMOS process. Fig. 7 shows a chip photograph and


Figure 4.   Truth table of (a) TDBA and (b) MRBA

X	Y	C_{out}	S_{out}
0	0	C	S_{in}
0	1	C	S_{in}
1	0	0	S_{in}
1	1	$C_{in} + S_{in}$	$\overline{C_{in} \oplus S_{in}}$

(a)

X	Y	C_{out}	S_{out}
0	0	C	S_{in}
0	1	C	S_{in}
1	0	$C_{in}S_{in}$	$C_{in} \oplus S_{in}$
1	1	$C_{in} + S_{in}$	$\overline{C_{in} \oplus S_{in}}$

(b)

performance summary of the proposed multiplier. The area of the proposed 8×8 multiplier is 9750 μm^2 and it consumes 145 μW at 1.2 V supply voltage when input patterns have 50 % probability of 0 and 1 with 50 MHz input frequency.

Fig. 8 shows the power comparison whether the TDBA and MRBA are used or not. Since the TDBA and MRBA have no FAs but ITBs to prevent logic evaluation when the logic is not used, they can achieve 33.7 %, 32.0 % power reduction, respectively, compared to the previous works [4, 6-7]. Fig. 9 shows the effect of the proposed OBA. When 8×8 parallel multiplier adopts the OBA, 15.7 % of power consumption can be reduced compared with the row-bypassing multiplier [4].

TABLE I represents the performance comparison with the previous works on bypassing multipliers. The power consumption of proposed multiplier is reduced by 15.7 % and 48.8%, compared to row-bypassing multiplier [4] and 2-dimensional bypassing multiplier [7], respectively.

V. CONCLUSION

A 145 μW 8×8 parallel multiplier is implemented in 0.13 μm CMOS process with 1.2 V supply voltage. The proposed multiplier adopts the OBA which consists of two kinds of adder cells, TDBA and MRBA, to reduce power consumption
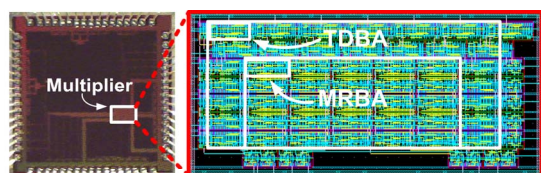
Process	Samsung 0.13 μm 1P6M CMOS
Area	150 μm X 65 μm (Core)
Supply Voltage	1.2 V
Power Consumption	145 μW @ 50 MHz input
Delay	~3 ns

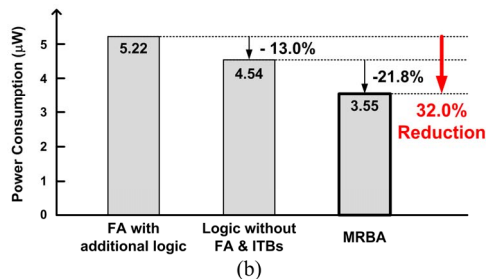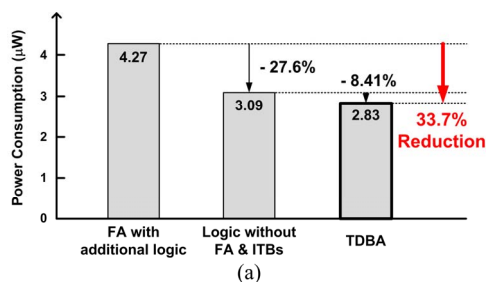Figure 7. Chip photograph and performance summary
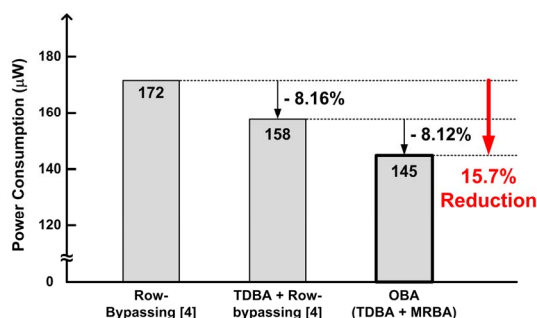
Figure 8. Power reduction results of (a) TDBA and (b) MRBA

Figure 9. Power reduction results by using OBA

TABLE I. PERFORMANCE COMPARISON

Design	Power (μW)	Normalize (%)
Braun	179	100
Row-bypassing [4]	172	96.1
Column-bypassing [5]	177	98.9
2-dimensional bypassing [7]	283	158
Proposed	**145**	**81.0**

with the bypassing scheme. The proposed OBA decreases power consumption by 15.7 % compared to the previous row-bypassing multiplier. The TDBA and MRBA don't use FAs and minimize the number of extra logic. Also, the TDBA and MRBA partially activate the logic evaluation by ITBs, so that their power consumption is reduced by 33.7 % and 32.0 %, respectively, compared to the FA with additional logics. As a result, 145 μW of power consumption is achieved in the 8x8 multiplier when the input frequency is 50 MHz and the probability of 0 and 1 of inputs are both 50 %.

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